Article

A TCAD Study on Simulation of κ-Ordered Stacking of Gate Oxide Dielectrics for FinFETs

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**Abstract:** In this paper, we present simulation results obtained using TCAD tools for a 3-D silicon on insulator (SOI) n-FinFET structure with various gate dielectrics with κ-ordered stacking in FinFET geometries. In conjunction with known studies on stacked laminates of gate-oxides like SiO2, Al2O3 and HfO2, this study further introduces and explores stacking of gate oxide laminates in increasing dielectric constant (κ) value, artificially forming a κ-graded functionally graded material (FGM). A numerical analysis, via introduction of a custom benchmark, is conducted to show viability of usage of these structures against conventional single layer high-κ dielectrics for FinFET structures. Impact of using such κ-ordered dielectric structure on key electrical performance parameters were analyzed with respect to the typical performance parameters, threshold voltage (**V**TH), on-state current (**I**ON), off-state current (**I**OFF), drain-induced barrier lowering (**DIBL**) and subthreshold slope (**SS**), **I**ON/IOFF ratio and gate metal-to-silicon leakage current (**IG**). Using SILVACO ATLAS for device simulation, single layer gate dielectrics SiO2, Al2O3, HfO2, La2O3 and TiO2 of 3 nm thickness (**t**ox) for a 14 nm channel (fin) length (**L**FET), 2 nm channel width (**W**FET), 5nm channel height (**h**fin) FinFET structure is analyzed as the control group. 13 different 2- or 3-stage κ-ordered FGM gate-oxide combinations, like [Al2O3:HfO2:TiO2], staged in parallel, connected serially. Modified Penn Model [1], [2] is used to calculate the dielectric constant of thin nanolaminate material forming each FGM laminate, using their bulk dielectric constant bandgap energy EG, high frequency dielectric constant and its Fermi wave vector *K*f. Maxwell-Garnet (MG) approximation [3] is selected to calculate the effective dielectric constant () for the 2-and 3-layered FGM dielectrics. Quantum tunneling model and Hot Electron / Hot Hole Injection (HEI-HHI) models [4] are used to model gate leakage current within SILVACO ATLAS/Deckbuild simulation tool and results were found to be consistent with experimental results within [5] with systematically varying thickness of mentioned dielectric layers to form a graded structured 3 nm-thickness FGM gate dielectrics. FinFET Buried Oxide (BOX) material was kept as Al2O3 through all simulations. [1], [2][3][4][5]Our results indicate that proposed FinFET with FGM gate dielectrics has lesser IGL up to 53 times, lesser DIBL up to %38.2, lesser SS up to %7.6, lower IOFF up to 2 decades, higher ION up to %62, higher ION/IOFF up to 45 times and lesser VTH up to %19.2, with respect to the FinFET of same dimensions composed of single layer HfO2 gate dielectric. FGMs show better performance than single material dielectric when used as gate insulating materials. Results may provide versatile opportunities for optimizing FinFET devices.

**Keywords:** Technology Computer-Aided-Design (TCAD) Simulation; stacked high-κ gate-oxide dielectrics, Functionally Graded Material (FGM); Junctionless Thin Film Transistor (JLTFT); Fin-Field Effect Transistor (FinFET); Drain Induced Barrier Lowering (DIBL); Subthreshold Slope (SS); Threshold Voltage (VTH); ION/IOFF ratio.

1. Introduction

Stacked laminates of gate-oxides on FinFETs have been investigated in several research papers. Lorenzo et.al proposed a gate engineered oxide stack silicon on insulator (SOI) FinFET device with a high-κ dielectric gate oxide stack structure, which improved the analog and RF performance of the device compared to standard single gate oxide structures [6]. Nigam et.al studied the reliability of stacked oxide heterogeneous gate dielectric polarity gate junctionless tunnel FET (PG JLTFET), which used a high-κ gate dielectric material (HfO2) layer on top of the silicon dioxide (SiO2) layer to improve device performance [7]. Gangwani analyzed the temperature performance of a stacked oxide top-bottom gated junctionless FinFET, which showed enhanced output performance and reduced short channel effects compared to conventional junctionless FinFET [8]. Das et.al proposed a dual-material-gate dual-stacked-gate dielectrics gate-source overlap Ge FinFET with low leakage current, high on drain current, and high ratio of on current to off current [9].

HfO2 thin films have wide band gap of ≈ 5.8 eV, high dielectric constant (κ ≈ 25) and suitable band offset values relative to Si substrate. In addition to their excellent thermodynamic and chemical stability, HfO2 has been strongest candidate material for replacing single layer SiO2 gate dielectrics. (reference koy) however, there exists no simple binary oxide dielectric between the κ greater than 35 (of Nb2O5) and less than 95 (of TiO2). Thus there starts the possibility and opportunity to generate materials with κ in the range of 35-95 through FGMs, that have the potential to show better performance properties than known gate-oxides, especially when a method to calculate the equivalent dielectric constant of the stacked FGM materials. Among existing methods Maxwell-Garnet equation [3] for calculation of effective κ for 2-layer dielectrics. As we need 3-layer effective κ calculation we need to derive the two equations for 3-layer dielectrics.

In this paper we introduce functional gate dielectrics consisting of 2- or 3- layer known dielectrics working on FinFETs, which might be candidate for fabrication on top of Si-channeled FinFETs. Similar work and simulations were addressed in papers [17], [18], [19].,

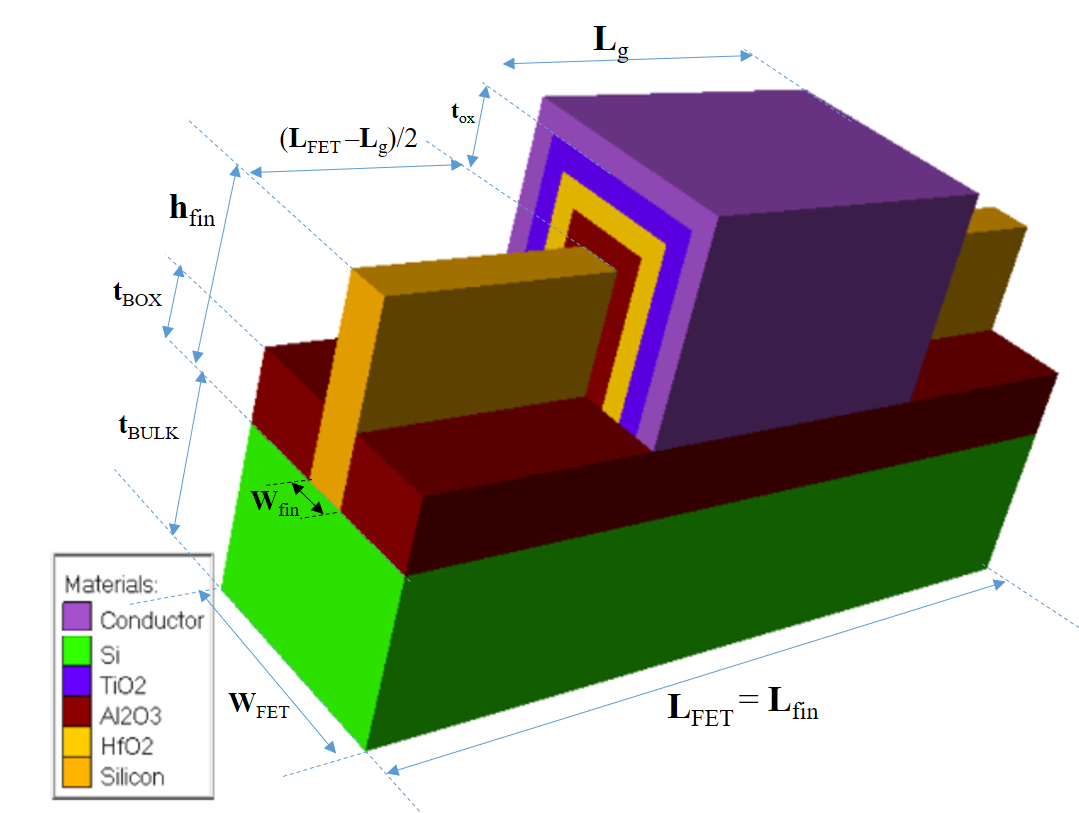
Modified Penn Model [1], [2] is used to calculate the dielectric constant of thin nanolaminate material forming each FGM laminate, using their bulk dielectric constant bandgap energy EG, high frequency dielectric constant and its Fermi wave vector *K*f. Maxwell-Garnet (MG) approximation [3] is selected to calculate the effective dielectric constant () for the 2-and 3-layered FGM dielectrics. Quantum tunneling model and Hot Electron / Hot Hole Injection (HEI-HHI) models [4] are used to model gate leakage current within SILVACO ATLAS/Deckbuild simulation tool and results were found to be consistent with experimental results within [5] with systematically varying thickness of mentioned dielectric layers to form a graded structured 3 nm-thickness FGM gate dielectrics. FinFET Buried Oxide (BOX) material was kept as Al2O3 through all simulations.

In this work, simulations were performed with single and double FGM dielectric materials for trigate FinFET structure. Our research focused on conducting a simulation-based study of FinFETs since their introduction in the year 2000 [20], performance of FinFET technology, including analytical modeling and simulation of FinFET devices [21], the influence of fin geometry on corner effects in multifin dual and tri-gate SOI-FinFETs [22], benchmarking of FinFET, nanosheet, and nanowire FET architectures for future technology nodes [23], the analog performance analysis of stacked oxide top-bottom gated junctionless FinFET [22] and a detailed study of single-material gate, double-material gate, and triple-material gate FinFETs were carried out [24]. In-depth analysis of typical types of FinFETs were presented in [25] with which we tried to match the terminology and abbreviations within that paper.

2. Device Structure

The 3D Technology Computer-Aided Design (TCAD) structure for FinFETs is shown in Fig. 1.

Using SILVACO ATLAS for device simulation, we start with SiO2, Al2O3, HfO2, La2O3 and TiO2 as single layer gate dielectrics of 3 nm thickness (tox) for a 14nm channel (fin) length (LFET), 2 nm channel width (WFET), 5 nm channel height (hfin) FinFET structure, then formed 13 different FGM materials with systematically varying thickness of mentioned dielectrics to form a graded structured 3 nm-thickness gate oxide dielectric. With thickness of 3 nm, BOX material (Figure 1) is kept as Al2O3 and never changed through simulations. Equal doping concentration of 5x1019 cm–3 is used source - drain channel region.



Buried Oxide (BOX) on Silicon

Gate

Channel

**Figure 1.** Proposed 3-material FGM gate oxide dielectric based FinFET

**Table 1.** Proposed FinFET properties.

|  |  |  |
| --- | --- | --- |
| Property | Value | Note / Abbreviation |
| Channel (Fin) Length | 14 nm | Lfin |
| Gate thickness | 10 nm | Tg |
| Channel (Fin) Width | 2 nm | Wfin |
| Gate Length | 14 nm | Lg |
| Fin Width | 2 nm | Wfin |
| Fin Height | 5 nm | Hfin |
| Channel Concentration | 5x1019 cm-3 | Nd |
| Gate work function | 5 eV | φw |
| FET Length | 34 nm | LFET |
| FET Width | 10 nm | WFET |
| Total Gate Oxide thickness | 3 nm | tox |
| BOX Thickness | 3 nm | tBOX |
| BOX material | Al2O3 | - |
| Bulk Si Thickness | 10 nm | tBULK |

3. Materials and Methods

As we target to prove that FGM gate oxide dielectric structures behave and perform better than single material dielectric structure in FinFET design, our method will be 5 steps. We need to analyze, model and evaluate the nanoscaled dielectric structures decreasing thickness will reduce the bulk capacitance and dielectric constant of the dielectric. First in IIIa, Modified Penn Model [1], [2] is used to calculate the dielectric constant of thin nanolaminate material forming each FGM laminate, using their bulk dielectric constant bandgap energy EG, high frequency dielectric constant and its Fermi wave vector *K*f. In part IIIb thru IIIc, Maxwell-Garnet (MG) approximation [3] is selected to calculate the effective dielectric constant () for the 2-and 3-layered FGM dielectrics. In IIId and IIIe, FinFET model in Figure 1 is implemented via ATLAS language and Hot Electron / Hot Hole Injection (HEI-HHI) model [4] is used to model gate leakage current within SILVACO ATLAS/Deckbuild simulation tools are used to calculate with experimental results within [5], with systematically varying thickness of mentioned dielectric layers to form a graded structured 3 nm-thickness FGM gate dielectrics. Eighteen different FinFET model simulationsare performed in Silvaco Atlas Deckbuild, first five models include single material gate oxide dielectrics in Table 4A and subsequent thirteen models include FGM dielectrics as gate-oxide (in Table 4B). Thru IIIf and IIIg, key electrical performance parameters like threshold voltage (**V**TH), on-state current (**I**ON), off-state current (**I**OFF), drain-induced barrier lowering (**DIBL**) and subthreshold slope (**SS**), **I**ON/IOFF ratio and gate metal-to-silicon leakage current (**IGL**) are selected and evaluated for each simulation. We also design a customized figure of merit in order to justly evaluate each FinFET performance with respect to each other. Here we present details each step as below:

3.1. Thickness Dependence of Under Quantum Confinement Effects

Theoretical foundation for constructing a -graded FGM is given in US Patent 8110469 by Gealy et.al. [26] and we model our gate oxide for FinFET as below:

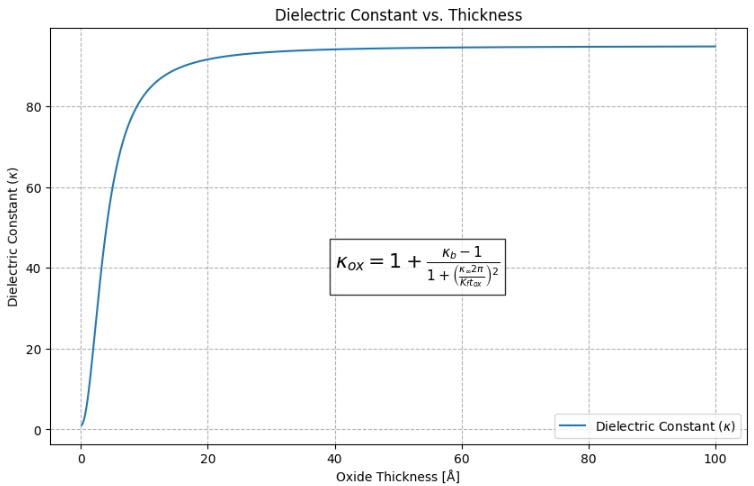
metin, diyagram, ekran görüntüsü, çizgi içeren bir resim

Açıklama otomatik olarak oluşturuldu

**Figure 2.** Stepwise Grading Profile for an example FGM (FGM-H in Table 4B.) as gate oxide dielectric.

Gate oxide dielectric constant has to be evaluated for according to the formula, Equation-1,

where is the bulk dielectric constant, is the high frequency dielectric constant, is Fermi wave vector, is the thickness of the nanoscaled dielectric material [1].

metin, diyagram, çizgi, öykü gelişim çizgisi; kumpas; grafiğini çıkarma içeren bir resim

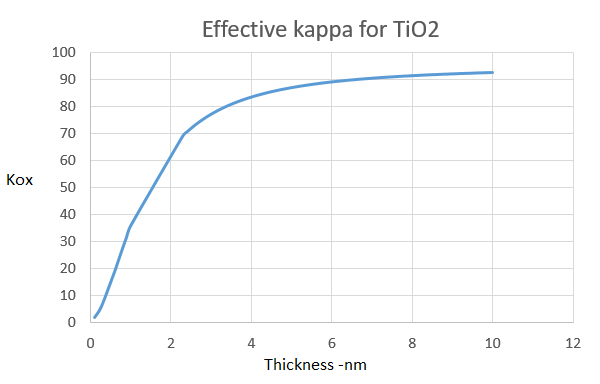
Açıklama otomatik olarak oluşturuldu

Iki grafiği tek grafikte birleştir ve yazılar daha okunur olsun.

**Figure 3.** Modified Penn Model for dielectric constant against thickness applied to TiO2 [1], [2].

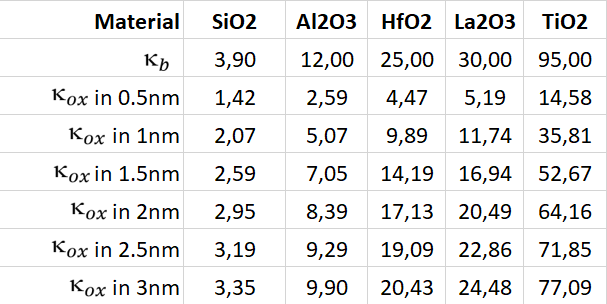
For silicon (Si), it has been shown that for thicknesses greater than 10 Å (1 nm), bulk can be considered to be unchanged and equivalent to [2]. If is less than 10 Å then we need to consider generalized Penn model [27] for modelling dielectric constant as against thickness, under quantum confinement effects for nanolaminates for each FGM’s to be calculated correctly. As we herein try to model nanolaminates around 5-30 Å, we calculated of interlayer nanolaminate according to Equation-1. This can be numerically further fitted to the Equation-2 in [27] ;

and when we calculate the resultant kappa of same material due to its nanolaminate thickness and observe the significant loss in dielectric effect when we observe Table-2. This numerical approximation is depicted in Figure 4, showing that in orders of few nanometers nanolaminate TiO2 thickness, kappa reduction is significant.



**Figure 4.** A numerical approximation for Penn Model evaluated by Equation-2.

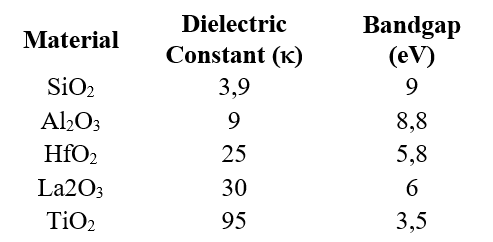
**Table 2.** Bulk dielectric constant and resultant oxide kappa with respect to nanolaminate thickness *tox* of dielectric materials calculated with Equation-2.



3.2. Modelling Oxide Nanolaminates as FinFET Gate oxide Dielectrics

In order to isolate the gate metal and form a proper electric field to control the drain current, gate dielectrics are of great importance. Dielectric constants (κ) of some selected gate oxides vary from 3.9 to 95 and their respective bandgaps vary from 9 eV down to 3.5 eV in Table 3.

**Table 3.** Bandgap and dielectric constant for simple binary oxides used in this paper [22], [23.]

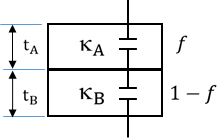


HfO2 thin films have wide band gap of ≈ 5.8 eV, high dielectric constant (κ ≈ 25) and suitable band offset values relative to Si substrate. In addition to their excellent thermodynamic and chemical stability, HfO2 has been strongest candidate material for replacing single layer SiO2 gate dielectrics. There exists no simple binary oxide dielectric between the κ greater than 35 (of Nb2O5) and less than 95 (of TiO2). Thus there starts the possibility and opportunity to generate materials with κ in the range of 35-95 through FGMs, that have the potential to show better performance properties than HfO2, especially when we utilize a method to calculate the equivalent dielectric constant of the stacked FGM materials. Among existing methods Maxwell-Garnet equation [3] for calculation of effective for 2 layer dielectrics. As we need 3-layer effective calculation we need to derive the two equations for 3-layer dielectrics as follows:

3.3. Derivations for 3-Stage FGM with Materials A,B,C

When two layers or phases of dielectric materials are deposited on top of each other, calculation of their effective or resultant dielectric constant of this serially connected sheets of two dielectric materials, also called as, effective dielectric constant for A-B material (effective ) would be calculated by two models, first by Maxwell-Garnet approximation model [3], [30] as Eq.2;

where are dielectric constants for material A and B and *f* is the volumetric filling factor for material A and (1 – *f* ) is the volumetric filling factor for material B in the two phase dielectric system of Fig 5.

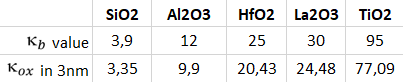


**Figure 5.** Two phase dielectric system connected in series.

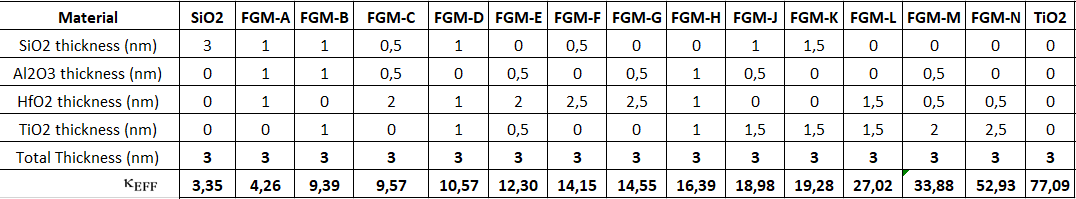
To extend this theory for a three-phase system, we need to consider additional complexities due to the interaction between three different dielectric materials. If we denote the dielectric constants of the three materials as ​​, ​ ​, and ​ and their respective volumetric filling factors as *f*A​, *f*B​, and *f*C​ with *f*A​ + *f*B​ + *f*C​= 1, we need to derive an expression that considers all three materials. Thus we can;

* Calculate the effective dielectric constant ​​ for materials A and B using the Maxwell-Garnett equation.
* Consider ​ as one material and apply the Maxwell-Garnett equation again with ​ and ​ to find the overall effective dielectric constant , with *f*A​B​ + *f*C​= 1, finally as Eq.3,

**Table 4A.** Control Group: Thickness and bulk values and calculated (modified Penn model) dielectric constants values of 5 single material gate dielectrics for 3 nm thickness.



**Table 4B.** FGM Group: Thickness and (applying modified Penn + MG model) values of 13 FGM gate oxide dielectrics between SiO2 and TiO2, shown as lower and upper limits of achievable within 3nm material thickness.



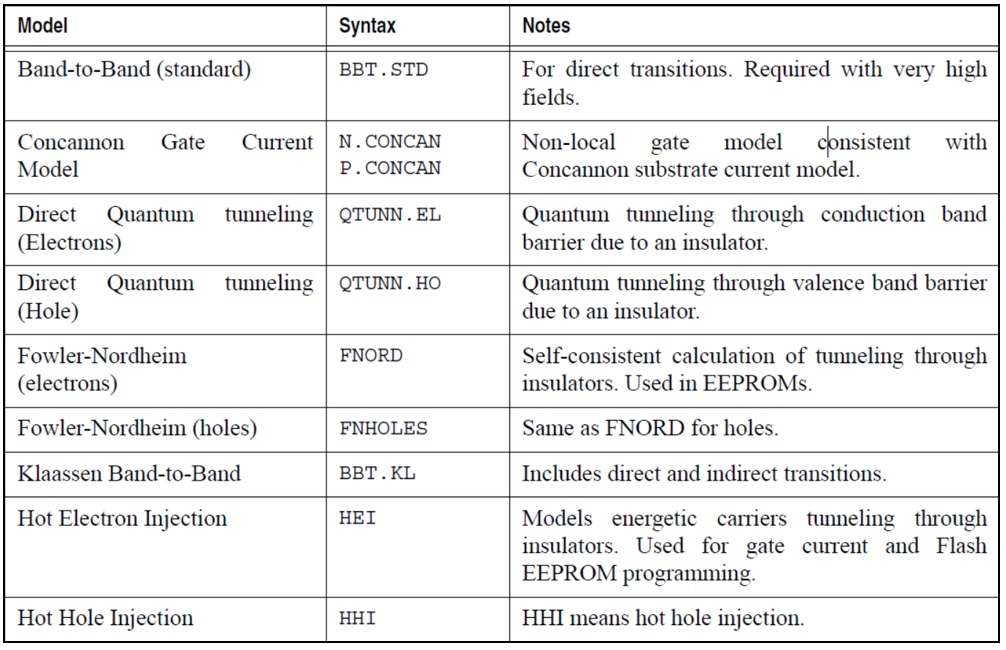
3.4. FinFET Modelling in Silvaco ATLAS Deckbuild Tool

We start with modeling our FinFET in Silvaco’s Atlas/Deckbuild. The family of such tools were used in many research to design and simulate the FinFET devices. The ATLAS Deckbuild simulation employing many standard recombination and continuity models like Shockley-Read-Hall, Schrödinger and Auger; used widespread for 2D/3D simulations of normal or heterogated single, double or triple-gated FinFETs [21],[24],[17].

3.5. Gate Leakage Current Modelling

In devices that have a metal-insulator-semiconductor (MIS) formation, the conductance of the insulating film would ideally be considered as zero. However, for the sub 0.5um generation of MOS devices there is considerable conductance being measured on the gate contacts [4]. In our case we used two lines of code for proper solvers to be activated in ATLAS/Deckbuild given in Appendix A, among tunneling-through-dielectric models available we used the hot electron/hole injection (HEI-HHI) tunneling model within ATLAS tool [4], so that gate-to-dielectric leakage current was properly and realistically modeled, which gave most accurate results comparable with [5].

**Table 5.** Summary of used models for tunneling and carrier injection for gate-dielectric leakage current in ATLAS [4.]



3.6. Choice of Performance Metrics

Our performance metrics were selected as:

* **IG**, On-state gate leakage Current, in Amperes, leaks from gate metal through dielectric into the channel, when VGS = 0.75V in our case, needs to be minimized.
* **ION**, On-state Drain Current, in Amperes, when VDS = VDD (=1.2V in our case) and VGS= VDD , needs to be maximized.
* **IOFF**, Off-state Drain Current, in Amperes, when VDS = VDD and VGS = 0.0V, needs to be minimized.
* **ION/IOFF Ratio**, unitless, accepted and powerful measure of TFT design quality, needs to be maximized.
* **VTH**, Threshold Voltage, in Volts, the minimum VGS voltage that drain current ID slightly exceeds a limit current (1x10-7 A in our case) significant for the design, needs to be minimized.
* **SS**, Subthreshold Slope, in mV/decade, change in the gate voltage required to decrease the drain current ID by one decade, SS = ∆VGS/∆log(ID) , needs to be minimized.
* **DIBL**, Drain-Induced Barrier Lowering, in mV/V, represents the drain voltage VDS influence on the threshold voltage VTH, defined as DIBL = |∆VTH|/|∆VDS| , needs to be minimized.

as these are the primary parameters for evaluation of thin film transistors’ performance. [31]

3.7. Selection Process for the FGM – Creation of a Custom Figure of Merit

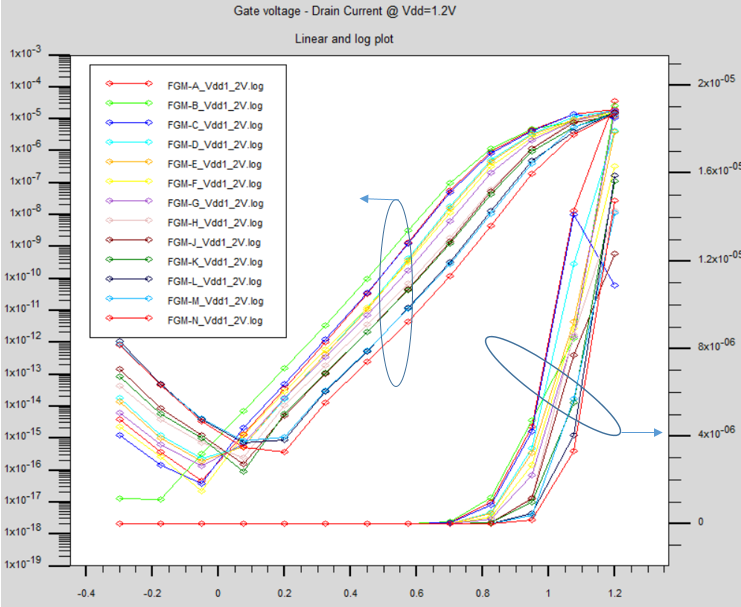
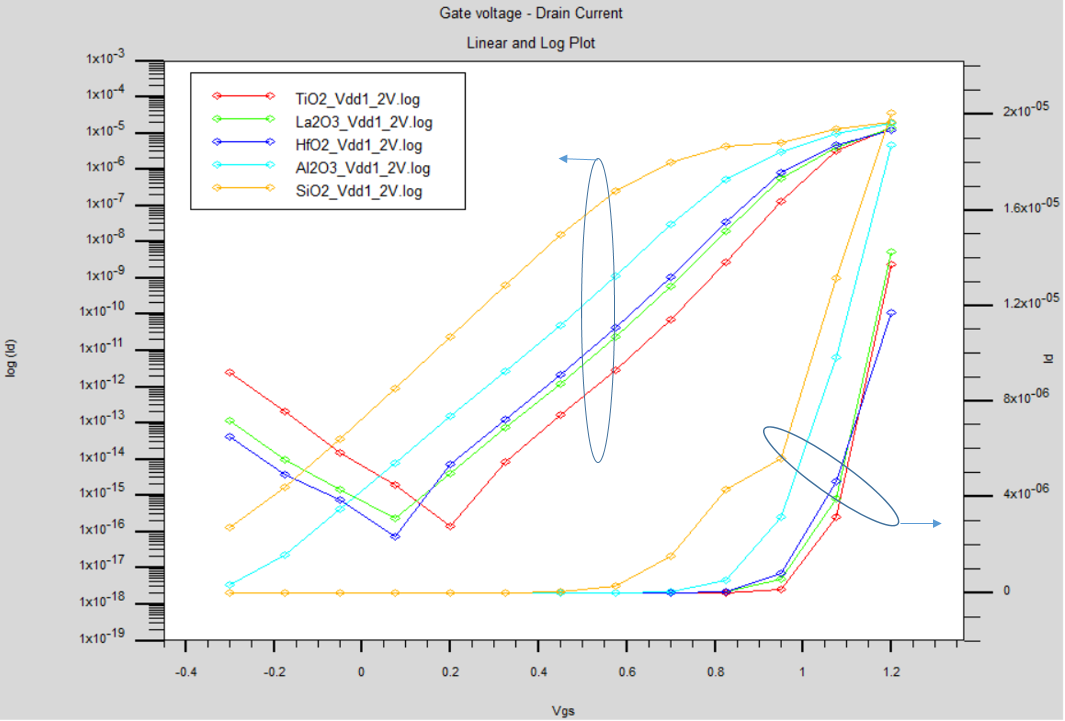
At the end of calculation process, we introduce and propose a unitless figure of merit as Equation-4:

with which we can evaluate the overall performance of FinFET under consideration. We developed this figure of merit that equally and mostly cares for IGL, ION/IOFF ratio and VTH, gives less importance to DIBL and even lesser importance to SS. Overall FOM value is multiplied by an arbitrary constant 97.62 to achieve best performing FinFET to appear with value equals to 100 and all other performance values to be normalized between 1 and 100. We compared the values of all single and FGM dielectric configurations so that it may help better to decide the selection among all configurations.

4. Results and Discussion

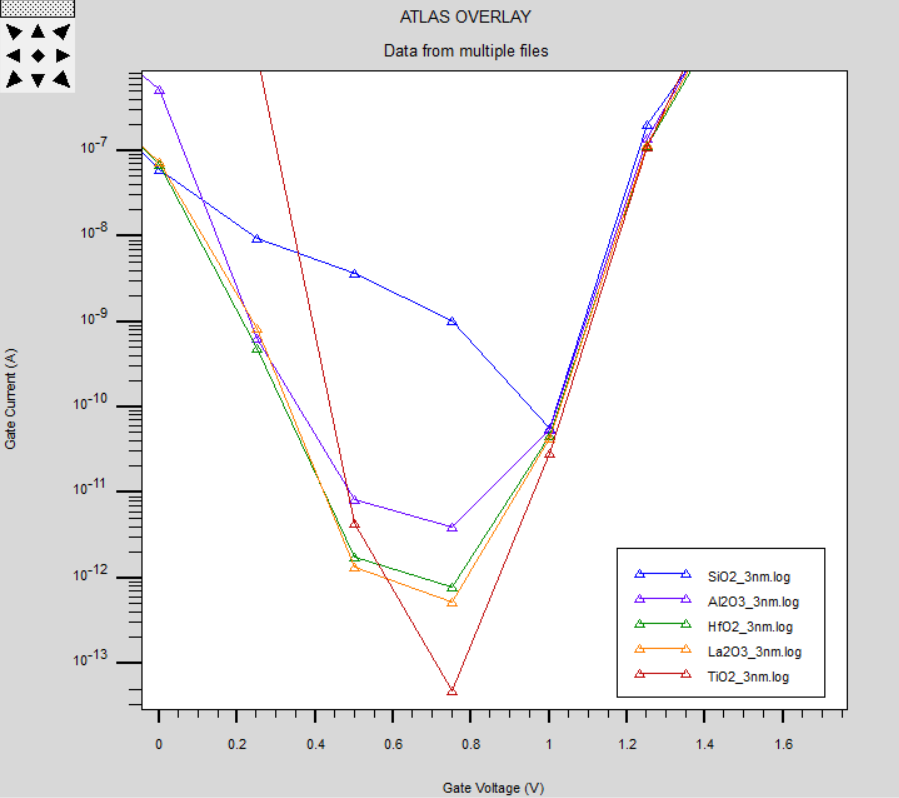
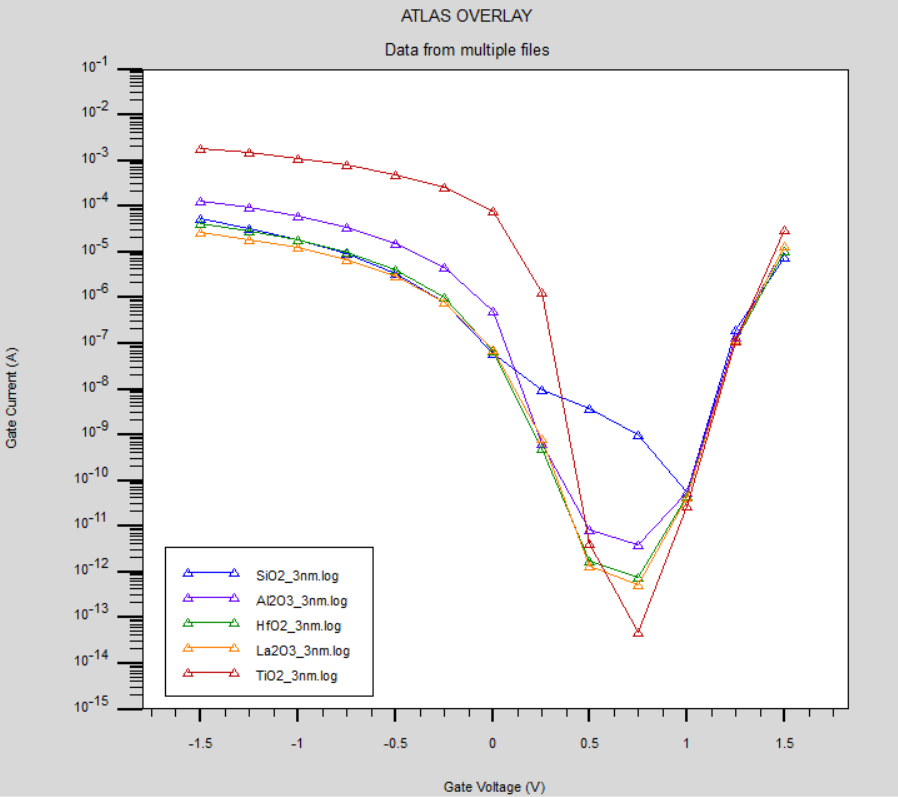
4.1. ID - VGS Transfer Characteristics

Figure 6. shows the drain current (Id) versus gate-source voltage (Vgs) characteristics for the FinFET device we examined with various gate dielectric materials. The threshold voltage is the point where the curve starts to steeply rise, which is a critical parameter for switching characteristics. The graph includes TiO2, La2O3, HfO2, Al2O3, and SiO2 as gate dielectrics. These materials are high-k dielectrics, with the exception of SiO2, which is a traditional dielectric material with a lower dielectric constant. TiO2 seems to have a higher on-current for the same gate voltage compared to the others, which may suggest better channel formation or a higher dielectric constant, which can modify the effective channel thickness. The choice of dielectric material significantly impact device performance. Higher-k materials like HfO2 and TiO2 may allow for thinner dielectrics, which can enhance gate control and reduce leakage currents, while also allowing for scaling down the device dimensions.

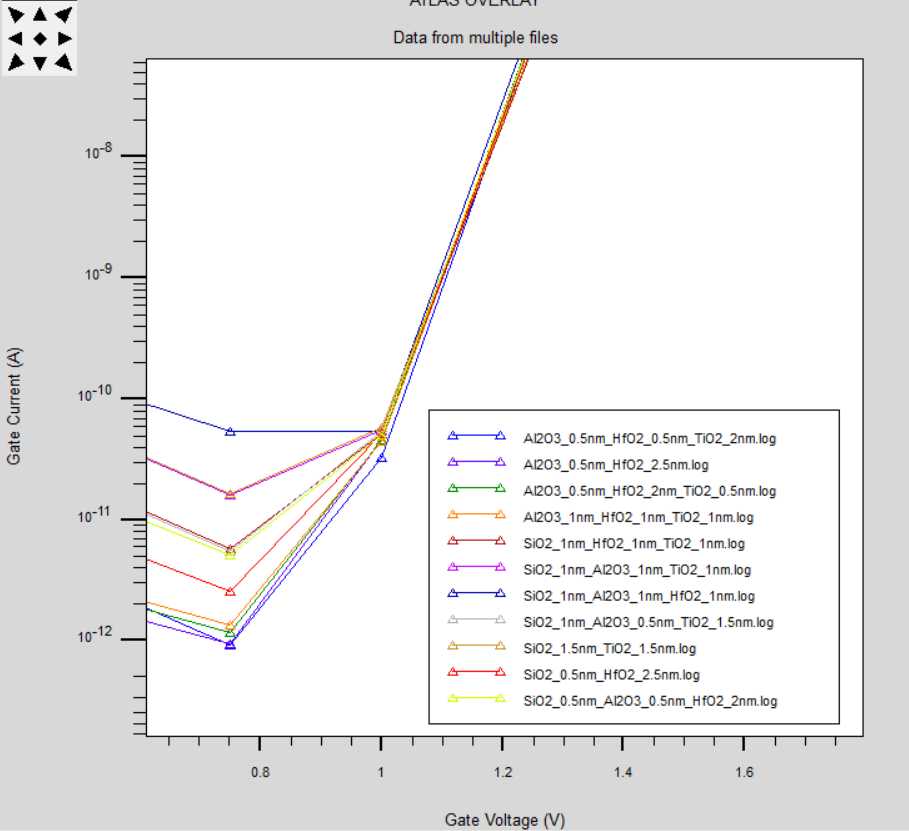
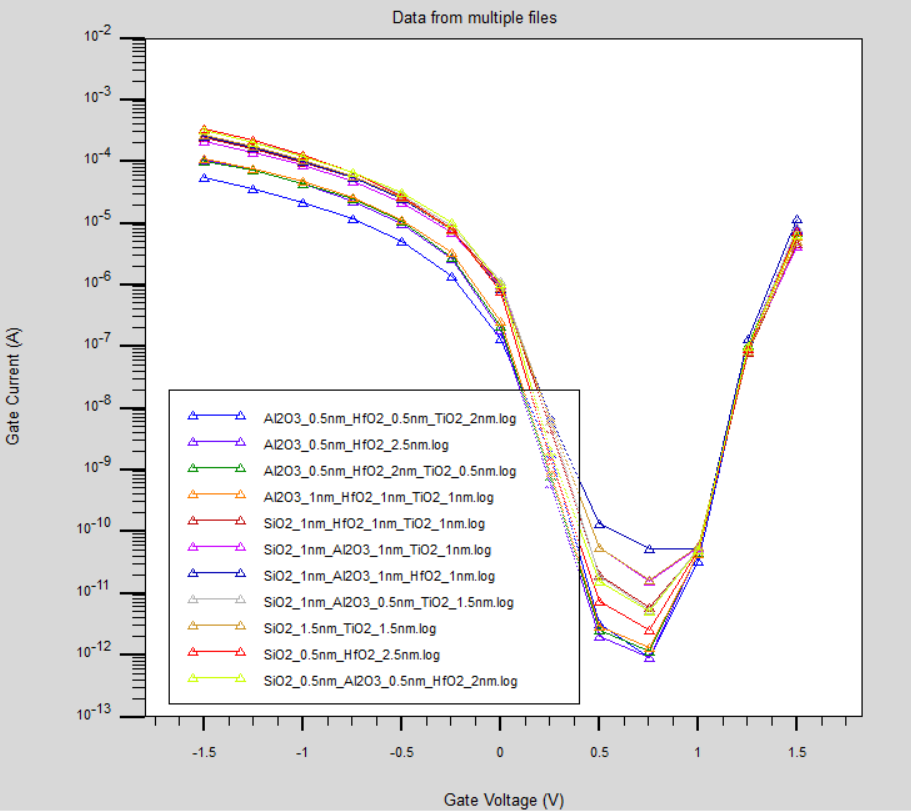


**Figure 6.** a. ID for single material gate oxide dielectrics (control group) log(ID) –VGS (left) and ID –VGS (right) b. ID current for FGM-group of gate oxide dielectrics log(ID) –VGS (left) and ID –VGS (right).

4.2. IG per VGS Leakage Current



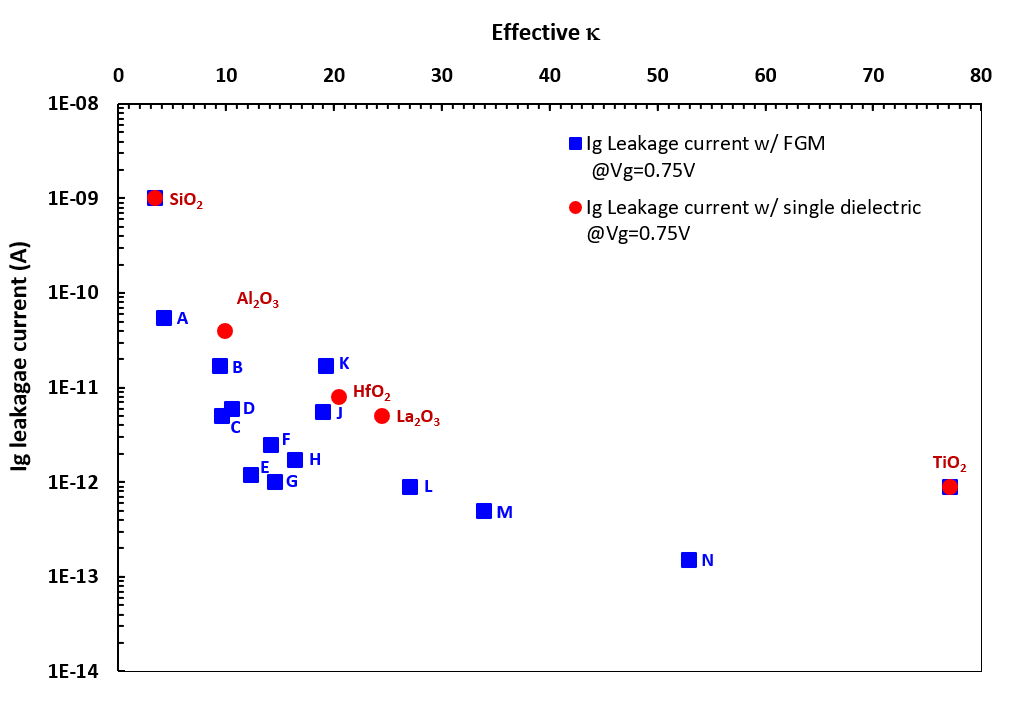
(a) (b)



(c) (d)

**Figure 7.** a, 7b (zoom): IG leakage current for single material gate oxide dielectrics (control group) log (IG) –VGS 7c, 7d (zoom): IG leakage current for FGM group gate oxide dielectrics, log (IG) –VGS.

This graph shows the leakage current characteristics in hot electron/hole injection model [4] for traditional single material gate dielectrics like TiO2 having least leakage current around 10-13 A at 0.75V for our specific FinFET under examination depicted in Figure 1. The curves generally show a similar trend, with this leakage current decreases with increasing gate-source voltage due to better formation of depletion region. The right graph displays the leakage current for FinFETs with FGM gate oxides, labeled FGM-A through FGM-N. The curves are closely grouped and follow a similar trend to the control group, but with some variation between the different FGM materials. Lower leakage current is preferable, especially for memory devices like EEPROMs where high IG can contribute to charge loss and memory degradation over time. The performance of FGMs in terms of IG appears similar to single-material dielectrics, suggesting that FGMs might provide not significant but slight advantage in reducing IG, but they also do not exhibit any deficiency in device reliability.

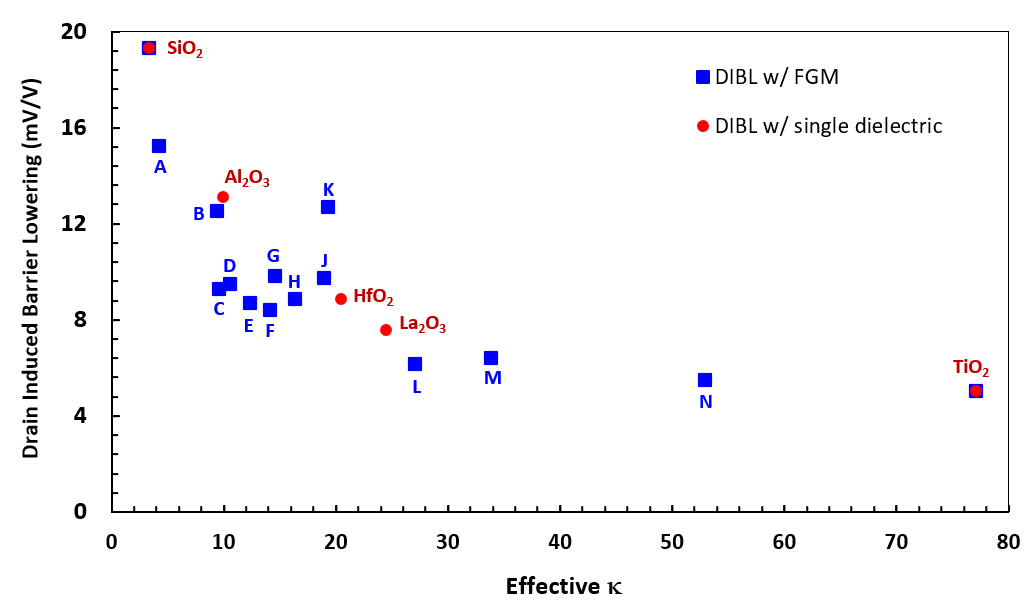


**Figure 8.** Ig Leakage Current for FinFET with single material and FGM gate oxide dielectrics (calculated with MG model).

We realize that usage of FGM dielectrics has potential of generating lower leakage currents from gate to channel, and for FGM-N, it is almost 53 times less than that of the FinFET with single HfO2 dielectric, as it becomes evident that interface effects minimize when smoother transitions of dielectric constant are fabricated starting from channel to gate material.

4.3. Drain Induced Barrier Lowering

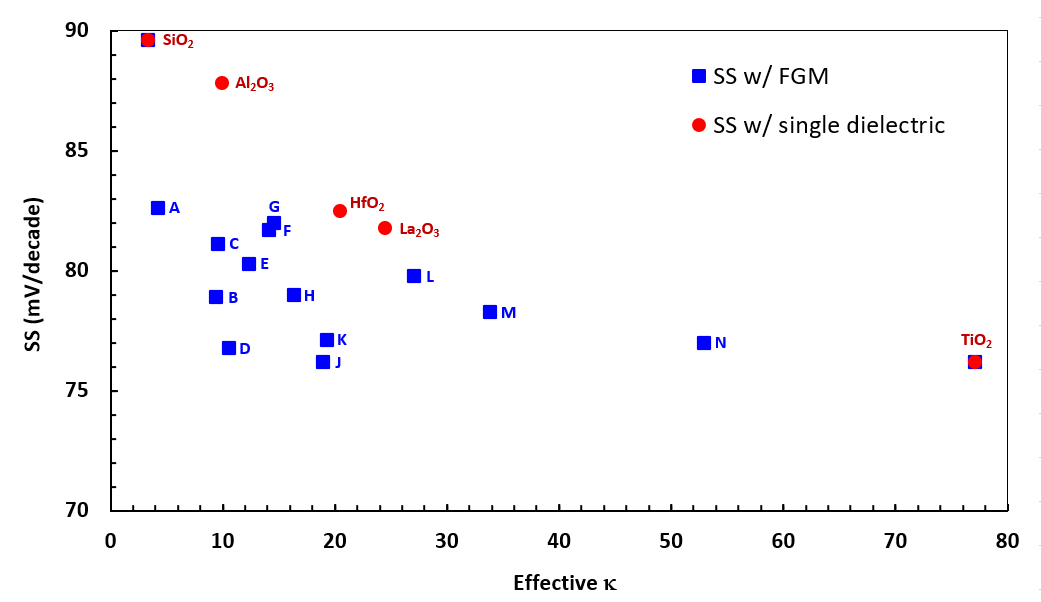
Figure 9 plots the Drain Induced Barrier Lowering (DIBL) against the effective dielectric constant (k) for different materials used in FinFETs. As DIBL is the short-channel effect where the drain voltage can influence the threshold voltage of the transistor, a lower DIBL value does generally better because it means the device has better control over the threshold voltage and is less susceptible to variations due to changes in the drain voltage. DIBL with single dielectric (Solid Line) represented the DIBL performance across a range of dielectrics for a standard single-layer dielectric material, starts high with SiO2 and then decreases significantly as the effective increases, showing improved performance for materials with higher κ values like HfO2, Al2O3, and TiO2. The trend suggests that as the effective dielectric constant increases, the DIBL effect decreases, which is a favorable outcome. DIBL values when using FGM techniques have peaks (labeled from A to N) that indicate where the DIBL is higher, possibly due to process variations, material properties or anomalies. DIBL performance of FGM’s seems best for FGM-N with 5.48 mV/V which is %38.2 lower than that of HfO2.



**Figure 9.** DIBL with single material and FGM gate oxide dielectrics

4.4. Subthrehold Slope

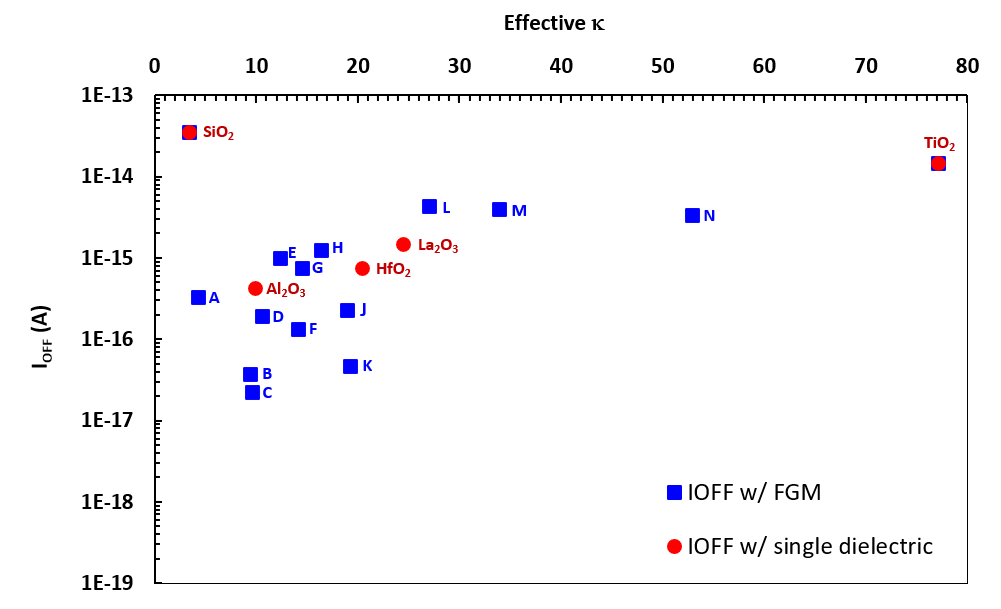
Subthreshold slope performance of FGM’s seems best for FGM-K with 76.2 mV/decade which is %7.64 lower than that of HfO2.



**Figure 10.** SS with single material and FGM gate oxide dielectrics

4.5. Off-State ID Current

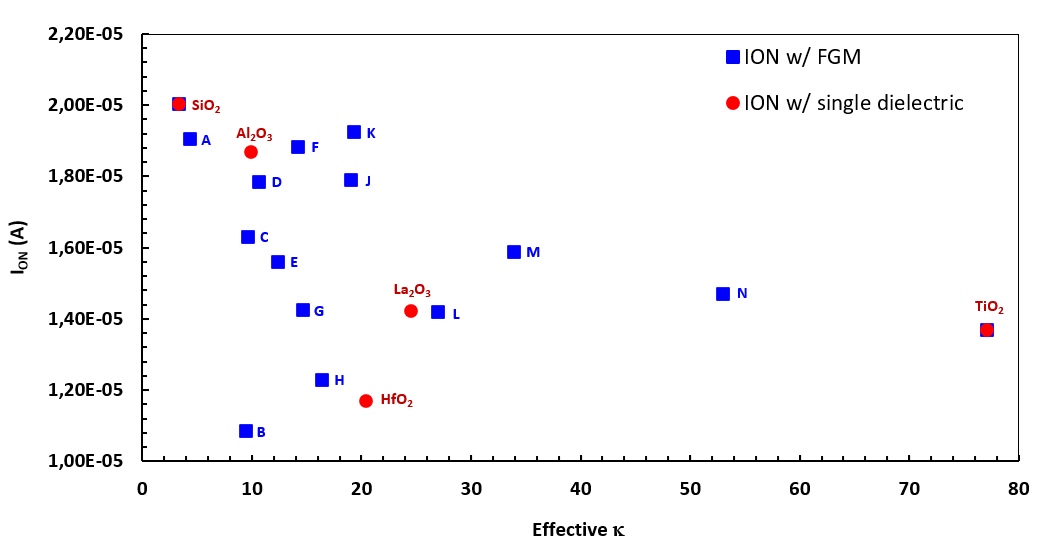
Off-State ID Current performance of FGM’s seems better for FGM-B with 2.23x10-17 A which is almost 2 orders of magnitude lower than that of HfO2.



**Figure 11.** IOFF with single material and FGM gate oxide dielectrics

4.6. On-State ID Current

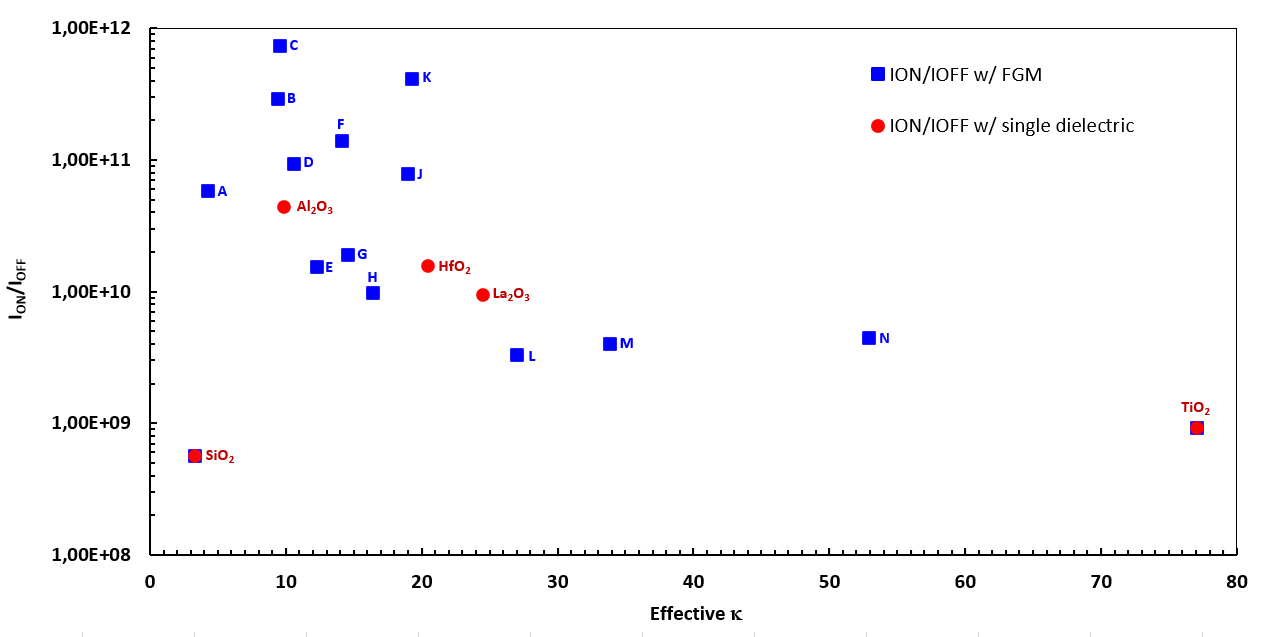
ON-State ID Current performance for FGM-K with 1.93x10-5 A which is almost %62 better than that of with HfO2.



**Figure 12.** ION with single material and FGM gate oxide dielectrics

4.7. ION / IOFF Ratio

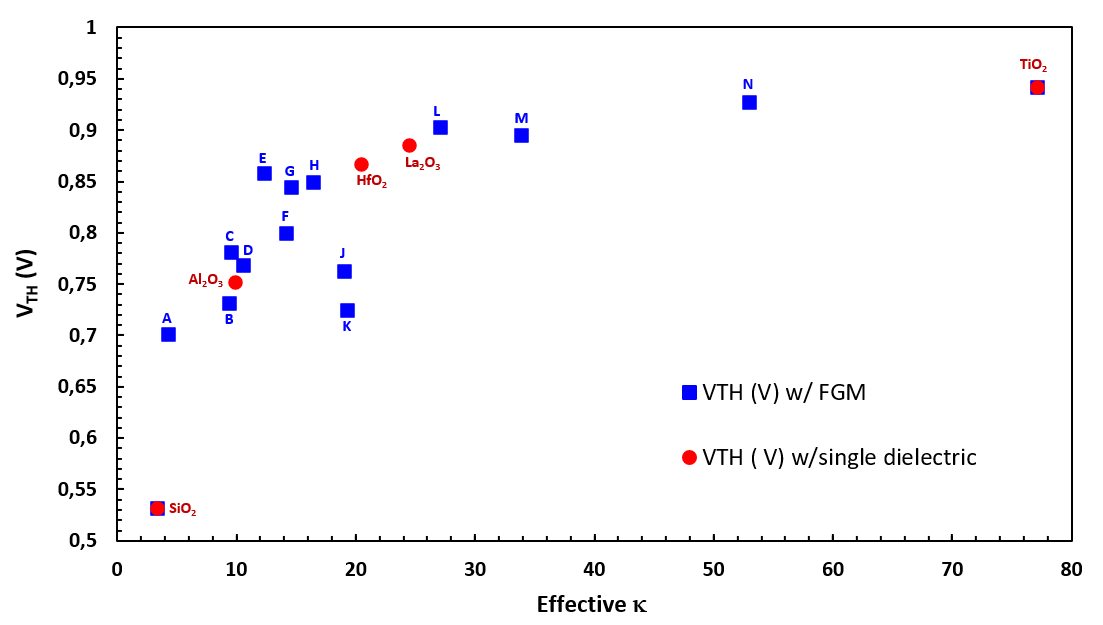
ION/IOFF ratio performance of FGM is better for FGM-C with 7.31x1011 which is almost 45 times better than that of HfO2.



**Figure 13.** ION/IOFF ratio with single material and FGM gate oxide dielectrics

4.8. Threshold Voltage VTH

VTH performance of FGM is better for FGM-A with 0.7012 V which is almost %19.2 better than that of HfO2.



**Figure 14.** VTH with single material and FGM gate oxide dielectrics.

5. Conclusion

The FGM technique may offer a way to engineer specific device characteristics, but it requires careful control and understanding of the material properties to achieve the desired outcomes consistently. Our results indicate that proposed FinFET with FGM gate dielectrics has lesser IGL up to 53 times, lesser DIBL up to %38.2, lesser SS up to %7.6, lower IOFF up to 2 decades, higher ION up to %62, higher ION/IOFF up to 45 times and lesser VTH up to %19.2.

**Table 6.**  values for each configuration of single dielectric and FGM configurations.

|  |  |
| --- | --- |
| **Material** | **FOM\_FET** |
| **SiO2** | **9,5** |
| **Al2O3** | **20,6** |
| **HfO2** | **33,4** |
| **La2O3** | **43,0** |
| **TiO2** | **76,0** |
| **FGM-A** | **20,0** |
| **FGM-B** | **70,2** |
| **FGM-C** | **70,9** |
| **FGM-D** | **38,4** |
| **FGM-E** | **45,6** |
| **FGM-F** | **38,0** |
| **FGM-G** | **58,0** |
| **FGM-H** | **41,6** |
| **FGM-J** | **40,3** |
| **FGM-K** | **56,1** |
| **FGM-L** | **65,9** |
| **FGM-M** | **69,3** |
| **FGM-N** | **100,0** |

Looking at the values calculated by Equation-4, single dielectric gate oxides TiO2 has the best performance. HfO2 performance achieved 33.4 whereas FGMs B, C, K, L, M and N achieve better than HfO2 and entire single material dielectrics except TiO2.

FGM approach aimed to improve the gate's control over the channel and seemed to achieve a success with respect to the FOMFET selected as a figure of merit for overall FinFET performance, which can be always be customized due to importance of the performance parameter selected by the designer.

FGMs seem to provide some space to engineer new gate oxides between dielectric constants 35-95 and at least to try these as gate dielectric material. With respect to the same FinFET with single layer HfO2 gate dielectric performance, most FGMs showed superior performance. Within gate insulators and BOX structures, FGMs may provide versatile opportunities for optimizing FinFET devices.

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